REMARKS

Applicant respectfully requests reconsideration of the application. Claims 1-52 and 54-58 are now pending. The examiner is correct, claim 53 was inadvertently omitted. Claims 1, 2, 10, 14, 19, 24, 25, 30, 39 and 50 are independent. The fee paid with the Response to Office Action of August 2001 covers the addition of claim 58.

The amendment to claim 19 corrects an inadvertent error. In the August 2001 Response to Office Action, the word "synchronously" was moved from one point to another in many of the other claims. However, in claim 19, the word was removed without being reinstated elsewhere in the claim, as was intended. Viewed in the context of the entire prosecution, the amendment is neither narrowing nor made for a substantial reason related to patentability.

I. Consideration of the Geppert reference

Applicant resubmits the Geppert reference for consideration under 37 C.F.R. § 1.56. MPEP § 2133.03(b)(IV)(B) reads as follows:

> **B. Nonprior Art Publications Can Be Used as Evidence ...**
>
> Abstracts identifying a product's vendor containing information useful to potential buyers such as whom to contact, price terms, documentation, warranties, training and maintenance along with the date of product release or installation before the inventor's critical date may provide sufficient evidence of prior sale by a third party to support a rejection based on 35 U.S.C. 102(b) or 103. *In re Epstein*, 32 F.3d 1559, 31 USPQ2d 1817 (Fed. Cir. 1994) (Examiner's rejection was based on nonprior art published abstracts which disclosed software products meeting the claims. The abstracts specified software release dates and dates of first installation which were more than 1 year before applicant's filing date.).

See also MPEP § 2128. The Examiner is correct, that the Geppert reference itself is not prior art. However, the MPEP requires that the Geppert reference be considered for what it indicates the prior art to have been before the § 102(b) critical date. Applicant is unaware of any provision of the MPEP that permits the Examiner to ignore the Geppert reference.

Applicant requests that the Examiner consider the Geppert reference, and indicate that consideration by initialing the enclosed Form 1449.

II. The purported rejection under 35 U.S.C. § 112 ¶ 2

The Action reads as follows:

> Claims 1-52 and 54-57 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
>
> With respect to all independent claims, it is not seen how likelihood of the existence of an alternate coding of instructions triggers an interrupt.

The nature of the Examiner's question is not understood. First, it is not the job of a claim to teach "how" something happens under § 112 ¶ 2 – that is the job of the specification under § 112 ¶ 1. MPEP § 2171 forbids a "mix and match" approach to examination. This purported rejection has no legal existence.

Further, claim 1 clearly recites an interrelationship between "likelihood of the existence of an alternate coding of instructions" and "[triggering] an interrupt." Claim 1, in pertinent part, recites as follows:

> 1. A microprocessor chip, comprising: ...
>
> table lookup circuitry designed to retrieve an entry from a table, ... each entry describing a likelihood of the existence of an alternate coding of instructions located in the respective corresponding address range, ...
>
> interrupt circuitry ... to synchronously trigger an interrupt in accordance with interrupt criteria ... the interrupt criteria being based at least in part on the table entry associated with the address of the instruction, ...

The table entries each "describ[e] a likelihood of the existence of an alternate coding of instructions located in the respective corresponding address range." The "interrupt circuitry" triggers an interrupt "based at least in part on the table entry."

Claim 1 is clear and definite. If a microprocessor has table lookup circuitry that retrieves table entries that "describ[e] a likelihood of the existence of an alternate coding," and the microprocessor triggers interrupts "based at least in part on the table entry" (along with the other limitations of the claim), then the microprocessor is within the claim. If a microprocessor raises interrupts but does not do so based on the contents of a table entry in the manner recited in the claim, the microprocessor is not within the claim. If a microprocessor has lookup circuitry to retrieve entries from a table as recited in the claim, but does not raise interrupts based on the table entries, the microprocessor is not within the claim. It is straightforward to identify those microprocessors that fall within the claim, and those that do not. Accordingly, the claim is clear and definite.

The Examiner's remarks have no applicability whatsoever to the other claims purportedly rejected. For example, independent claims 2, 10, 39 and 50 recite neither "alternate coding" nor "triggering an interrupt."[5]

Applicant requests that the Examiner be more careful to (a) consider each individual claim on its merits, and (b) apply the law as it is set out in the MPEP.

III. Claims 2, 10, 39 and 50

The Action purports to reject claim 2 over the combination of Morley '982 and Woods '032. Claim 2, as amended in August 2001, recites as follows:

> 2. A method, comprising the steps of:
>
> as part of the basic instruction cycle of executing an instruction of a non-supervisor mode program executing on a computer, consulting a table, the table being indexed by the address of instructions executed, entries of the table containing attributes of instructions whose addresses index to the respective entries; and
>
> controlling an architecturally-visible data manipulation behavior or control transfer behavior of the instruction based on a content of a table entry associated with the address of the instruction.

Claim 2 recites a table whose entries are "indexed by the address of instructions executed." The Action points to col. 1, line 43 of Morley '982 as showing a dispatch table "indexed by the addresses of instructions." (Action of December 2001, page 3, lines 13-14).

The Examiner misreads Morley '982. The indicated portion of Morley '982 discusses a conventional software emulator (see the Title of Morley '982, and note that col. 1, line 43 lies in the Background of Morley.) Consider how a software emulator works. Imagine, for example, that a "Branch" instruction has the value 71, and a "Load Address" instruction has the value 65. Anytime the instruction value 71 is fetched for emulation, the emulator will index to entry 71 of the dispatch table, which will dispatch execution to the emulation code for Branch. If that same location is overwritten by the value 65 (e.g., by self-modifying code), then the program will change behavior – next time the same location is executed, the emulator will index to entry 65 of the table, and execute the code for Load Address. The value 71 will always cause a Branch, at

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[5] A few of the claims recite either "alternate coding" or "triggering an interrupt," but no other independent claim recites both.

whatever address it appears. The value 65 will always cause a Load Address, at whatever address it appears.

Thus, the table entries indicated by the Examiner are "indexed" by the value of a memory location. The address of the "instruction" is entirely irrelevant to the process of indexing into Morley's dispatch table.

The Office Action points to Morley '982, col. 1, line 43, for the single word "addressed," considered in isolation from the rest of the claim. Leaving aside the impropriety of a failure to consider all limitations of the claim rather than a single word, careful reading of Morley '982 reveals that the word "addressed" here is the address of a table entry, not the "address of the instruction," as recited in claim 2.

Thus, the dispatch table of Morley's Background is indexed by the value of an instruction, that is, the contents of a memory location, not by the address of the instruction (as recited in claim 2). This is true not only of the implementation discussed in Morley's Background, but the implementation discussed in the body of Morley's Detailed Description of the Invention (see Morley '982 at col. 4, lines 27-35; col. 5, lines 59-62; col. 5, lines 21-31).

There is no correspondence between the "table ... indexed by the address of instructions executed" of claim 2 and the "dispatch table" of claim Morley '982.

Claims 10, 39 and 50 are patentable for similar reasons.

IV. Claims 14 and 24

Claim 14 recites as follows:

> 14. A microprocessor chip, comprising:
>
> instruction pipeline circuitry;
>
> address translation circuitry; and
>
> a lookup structure having entries associated with corresponding address ranges generated by the instruction pipeline circuitry and translated by the address translation circuitry, the entries describing a likelihood of the existence of an alternate coding of instructions located in the respective corresponding address range.

The § 103(a) portion of the Office Action makes no attempt whatsoever to show that the underlined claim limitation is met by the prior art.[6] Consequently, there is no § 103(a) rejection of claim 14.

Section VI of the specification, "Statistical probing," discusses the PFAT (page frame attribute table) 172.[7] Entries of PFAT 172 correspond to memory pages. Each PFAT table entry includes five bits 624 (see Fig. 6b) that indicate, in an approximate, statistical way, the "likelihood of the existence of an alternate coding of instructions" on the corresponding page (*e.g.*, section VI.B (pages 101-103), section VI.C (pages 103-106), section VI.D (pages 106-111). PIPM 602 is used to resolve the uncertainty remaining after consulting the statistical information stored in bits 624 of PFAT 172.

None of the prior art tables behave in this manner. Both the dispatch table of Morley's Background and Table 16 contain the addresses of instruction sequences (Morley '982, col. 1, lines 40-65; Morley '982, col. 5, lines 59-62), not an "indication of the likelihood" of whether "an alternate coding of instructions" exists at all, as recited in claim 14. Accordingly, claim 14 is patentable over the art.

The Office Action contains no indication of whether Morley '982, Woods '032, or Bianchi '029 is relied upon to meet this limitation of the claim. To avoid "misleading" the Examiner (see section VII of this paper), Applicant will refrain from discussing the other references until the Examiner indicates which references were intended to be relied upon.

Claim 24 is patentable for similar reasons.

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[6] Applicant questions why the Office Action discusses the correspondence between the claim and the specification here. This is a *non sequitur* in the context of a § 103(a) rejection, and no substitute for a comparison of the claim to the prior art.

[7] Applicant notes an inadvertent error in the August Response, directing the Examiner's attention primarily to PIPM 602. PFAT 172 is a better example. The PFAT and PIPM are generally discussed in the same figures and sections of the specification, so the indications of section IV.B of the August Response are partially correct. The third paragraph of the Introduction (section I) of the August Response is also correct, in indicating that "The probe bits 624 of a single PFAT entry give an approximate indication, a likelihood estimate, of whether there is a translated code segment for any of the code in the region corresponding to the PFAT entry."

V. Claim 25

Claim 25 recites as follows:

> 25. A method, comprising the steps of:
>
> as an integral part of processing an instruction in instruction pipeline circuitry of a computer, consulting a lookup structure of entries, each entry corresponding to an address range translated by address translation circuitry, and describing a likelihood of the existence of an alternate coding of instructions located in the respective corresponding address range; and
>
> as a result of the consulting, changing an instruction set architecture under which instructions are interpreted by the computer.

The Office action nowhere specifically addresses itself to claim 25. There is no rejection of claim 25.

The Office Action obliquely addresses claim 25, stating that "Interrupt is an inherent process of an emulator because control of the pipeline is switching between two ISA's." "Inherency" is discussed in MPEP § 2112:

> **2112 Requirements of Rejection Based on Inherency; Burden of Proof**
>
> ...
>
> EXAMINER MUST PROVIDE RATIONALE OR EVIDENCE TENDING TO SHOW INHERENCY
>
> The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. ... "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.
>
> ...
>
> In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.

The Office Action makes no attempt to "provide a basis in fact and/or technical reasoning to reasonably support" any assertion of "inherency." Because the Office Action fails to comply with minimum requirements set out in the MPEP, any purported rejection is incomplete, and non-existent.

Further, the Examiner's reading of Morley '982 is incorrect. Morley '982 discusses a "software emulator" (Abstract; col. 1, line 7-12: "CPU is designed to execute a particular set of

software instructions."). Morley is directed to emulation on a CPU that executes only one ISA. If Morley had a single pipeline that was capable of executing two different ISA's, there would be no need to provide a software emulator for the emulated architecture. There is no support in Morley '982 for the assertion that "control of [Morley's] pipeline" causes "switching between two ISA's."[8]

VI. Claims 19 and 30

As now amended, claim 19 recites as follows:

> 19. A microprocessor chip, comprising:
>
> instruction pipeline circuitry; and
>
> interrupt circuitry cooperatively designed with the instruction pipeline circuitry to trigger an interrupt on execution of an instruction of a process in accordance with synchronous interrupt criteria, the interrupt criteria being based at least in part on a memory state of the computer and the address of the instruction, wherein the architectural definition of the instruction in an emulated architecture does not call for an interrupt.

The Action discusses claim 19 as follows:

> Merely the fact that Morley teaches an emulator is sufficient to meet the limitations of broad claim 19. See the term "jump in line 42 and 58 of column 1 and how the dispatch table is indexed by the instruction address in lines 40-65 of column 1. Further, even the convention interrupt in response to external events alone (the architectural definition – does not call for an interrupt) taught in Morley is sufficient of the rejection of broad claim 19.

The written rejection fails to make any *bona fide* attempt to examine *this claim*. The claim does not recite "an emulator" – the Examiner's reference to an "emulator" is simply irrelevant. Nor does the claim recite an "interrupt" in isolation, it recites a specific interrupt – an interrupt "based at least in part on a memory state of the computer and the address of the instruction, wherein the architectural definition of the instruction in an emulated architecture does not call for an interrupt." The written rejection nowhere discusses either the "memory state of the computer" or the "address of the instruction" as recited in claim 19. Because the written rejection omits discussion of much of this claim, <u>there is no rejection of claim 19</u>.

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[8] In the Office Action of April 2001, the Examiner stated that "[An] interrupt handler which is commonly for handling interrupt is recited for changing ISA." The current rejection for "obviousness" is somewhat incompatible with the Examiner's previous surprise at this claim limitation.

The discussion of claim 19 in the Office Action is too unclear to permit a real response – there is no comparison between any word of the claim and a specific point in any reference. For another example, there is no comparison of the word "jump" (3rd line from the bottom of page 3) to any claim limitation – Applicant is not sure what claim limitation is thought to correspond to the word "jump." Applicant suggests that any future rejection be set out in the form of a word-by-word comparison of the claim to the prior art, as recommended by the Patent Academy and the Board of Patent Appeals. *See, e.g., Ex parte Braeken*, 54 USPQ2d 1110, 1112-13 (Bd. Pat. App. Interf. 1999).

In an attempt to be helpful and move the case forward, Applicant points out that Morley '982 fails to discuss interrupt circuitry that meets the claim limitations. Morley '982 mentions the word "interruption" at four points – col. 4, line 63, col. 5 lines 36 and 37, and col. 8, lines 6-7. The written rejection makes no attempt to tie any one of these four occurrences to the limitations in the claim. Further, read in context, Morley's discussion of interrupts is entirely conventional – apparently Morley's interrupts are conventional timer interrupts or disk completion interrupts. There is nothing to suggests that the interruptions in Morley '982 are triggered by "an instruction ... wherein the architectural definition of the instruction in an emulated architecture does not call for an interrupt," let alone based on the conditions recited in the claim.

Claim 30 is patentable for similar reasons.

VII. "Misleading"

On page 3, line 18 of the December Action, the Examiner states that Applicant's discussion of the prior art was "misleading." This is a very serious charge: as the Examiner must know, any attempt to mislead could potentially render any issued patent unenforceable, pursuant to the "duty of candor and good faith" of Rule 56.

The Examiner criticizes Applicant for "[referring] to the portion of the Morley reference which the Examiner does not rely on for the rejection." But that is the entire problem: the April Action relied on no portion of any reference for entire paragraphs of each independent claim. The April Action was entirely silent on, for example, the "indexed table" of claim 2. Because there was no indication in the Action whether the Examiner intended to rely on Morley '982 or Woods '032 for the "indexed table," Applicant attempted to effectively advance prosecution by

showing of the difference between the claim and the "closest" portion of the references. The only alternative would have been for Applicant to say nothing – which would have been as destructive to progress of the prosecution of this application as the Examiner's own silence.

The Examiner's complaint is occasioned solely by his own piecemeal examination, not by any "misleading" by Applicant.

Because the Examiner's charge has such serious consequences, and is entirely baseless, Applicant must insist that the Examiner state on the record that the charge is entirely withdrawn.

VIII. "Identifying differences between the references and the claims"

At page 3, lines 1-8, the Examiner indicates that "Applicants fail to identify any defference [sic] between the references and the claims and to explain how the claims are patentable over the prior art. The Examiner is simply incorrect: the previous Response to Office Action clearly states the difference between each independent claim and the prior art. For example, claim 2 is contrasted to the art at page 23, lines 23-25. Claim 10 is contrasted to the prior art at page 24, lines 16-18. Claim 14 is contrasted to the prior art at page 26, lines 5-13. Claim 19 is contrasted to the prior art at page 25, lines 5-9. For all other independent claims, the Response indicates that the claim is patentable for analogous reasons.

The Examiner is requested to search his own soul to consider whether he is examining this application in good faith, or delaying it.

IX. Remarks of page 4 of the Office Action

At page 4, line 9-10, the Examiner states, "All independent claims (see claims 30 and 19 for example) merely broadly recite an interrupt circuit." The Examiner misrepresents the claims. The recitation of "interrupt circuitry" of claim 1, for instance, is one-hundred twenty-four words long. The recitation of "interrupt circuitry" in claim 19 is sixty-five words long. The "interrupt" of claim 30 is limited in a phrase of thirty-five words. To ignore all but two of those words and focus on only "broadly an interrupt circuit" can only be construed as an intransigent refusal to examine the claims, not a good faith performance of the Examiner's duties.

The remaining comments in this paragraph are similarly misguided, failing to discuss the particular limitations recited in the dependent claims. A number of dependent claims recite limitations that are entirely ignored in the Office Action.

Prosecution cannot advance when the Office Actions fail to consider the claims on their merits.

In any future rejection over the prior art, the Examiner is invited to (a) discuss the particular words of particular claims, rather than loose paraphrases of the claims, (b) indicate a particular point in some reference that is being relied upon, and (c) provide some "basis in fact and/or technical reasoning to reasonably support" the correspondence. Prosecution cannot advance when claims are rejected based on unsupported assertions. The Examiner apparently finds it difficult when Applicant attempts to respond to points that the Examiner should have raised, but did not. Properly-supported element-by-element rejections will reduce both these difficulties.

In view of the amendments and remarks, Applicant respectfully submits that the claims are in condition for allowance. Applicant requests that the application be passed to issue in due course. The Examiner is urged to telephone Applicant's undersigned counsel at the number noted below if it will advance the prosecution of this application, or with any suggestion to resolve any condition that would impede allowance. In the event that any extension of time is required, Applicant petitions for that extension of time required to make this response timely. Kindly charge any additional fee, or credit any surplus, to Deposit Account 50-0675, Order No. 5231.16.

Respectfully submitted,

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